claims renumbered as shown

17. The flash memory system of claim 16 and further including a plurality of select lines, each select line coupled to a control gate of a select transistor of the plurality of select transistors.

18 16. The flash memory system of claim 17 wherein the array of floating gate memory cells is located between the first multiplex circuit and the second multiplex circuit.

19 17. The flash memory system of claim 16 wherein the plurality of select transistors are located at opposite ends of the array of floating gate memory cells.

20 18. The flash memory system of claim 15 wherein the plurality of local bit lines are located on a different level than the plurality of global bit lines.

21 19. The flash memory system of claim 15 wherein at least one local bit line of the plurality of local bit lines is located above a drain diffusion region.

22 ~~20~~ 3. The flash memory system of claim 15 wherein the array of floating gate memory cells is arranged in rows and columns.